REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed July 27, 2004. Reconsideration and allowance of the application and pending claims are respectfully requested.

I. Claim Rejections - 35 U.S.C. § 102(b)

A. Rejection of Claims 1-3, 5-6, 9-15, 18, 21, 24, 30, 32, and 34

Claims 1-3, 5-6, 9-15, 18, 21, 24, 30, 32, and 34 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Widdershoven (U.S. Pat. No. 6,313,502). Applicant respectfully traverses this rejection.

It is axiomatic that "[a]nticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." W. L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983)(emphasis added). Therefore, every claimed feature of the claimed invention must be represented in the applied reference to constitute a proper rejection under 35 U.S.C. § 102(b). In the present case, not every feature of the claimed invention is represented in the Widdershoven reference. Applicant discusses the Widdershoven disclosure and its applicability to Applicant's claims in the following.

1. The Widdershoven Disclosure

Widdershoven discloses a semiconductor device comprising a non-volatile memory which is erasable by means of UV radiation. As is described by Widdershoven, the semiconductor device is formed as a floating gate transistor T that includes (i) an n-type source 7, (ii) a p-type drain 8, and (iii) a gate including a floating gate 9 and a

control gate 10. Widdershoven, column 4, lines 4-22. Accordingly, Widdershoven discloses three-terminal memory cells.

As is further disclosed by Widdershoven, the erasing of the semiconductor device is achieved by irradiating the device with UV radiation *in combination with* a "photovoltage that is generated during the UV irradiation which is applied to the control gate of the memory cells and which induces a field in the gate structure which counteracts the supply of electrons to the floating gate." Widdershoven, column 4, lines 49-55. This photovoltage is provided with "means 12," which is described as a "photodiode formed by an n-type surface zone 13 which forms a photosensitive pn junction 14 with the p-type surface region 5." Widdershoven, column 4, lines 55-58; Figure 2. Accordingly, the Widdershoven memory cells *include* erasing circuitry.

2. Applicant's Claimed Inventions

Beginning with claim 1, Applicant recites (emphasis added):

> 1. A system comprising:
>
> a high-density non-volatile fast memory ***having no erasing circuitry***; and
>
> an ultraviolet (UV) light window adapted to expose the high-density non-volatile fast memory to UV light.

Applicant notes that, contrary to that Widdershoven does not disclose or suggest a high-density non-volatile fast memory "having no erasing circuitry", as is required by claim 1. As is described above, Widdershoven teaches the opposite: Widdershoven's memory cells include a photodiode that generates a photovoltage during UV irradiation of the memory cell to prevent under-erasure of the memory cell. Therefore,

Widdershoven not only fails to teach a memory having no erasing circuitry, Widdershoven further *teaches away* from a memory cell that comprises no erasing circuitry. Indeed, the addition of the photodiode to Widdershoven's memory cell appears to be the focus of the Widdershoven disclosure. In view of the above, Widdershoven does not anticipate claim 1, or claims 2-3 which depend therefrom.

With particular reference to dependent claim 3, Applicant notes that Widdershoven fails to disclose a "two-terminal drain-gate-connected modified flash cell". As is described above, Widdershoven's memory cell is a three-terminal memory cell. Furthermore, Widdershoven suggests no two-terminal arrangement.

Regarding independent claim 5, Widdershoven does not disclose "two-terminal drain-gate-connected modified flash cells having no erasing circuitry" for reasons discussed in the foregoing. Specifically, Widdershoven does not anticipate two-terminal memory cells, or memory cells that have no erasing circuitry.

With respect to independent claim 10, Widdershoven does not disclose "modified flash cells having no erasing circuitry" for reasons discussed above in relation to independent claim 1.

Referring next to independent claim 30, Widdershoven does not disclose "erasing the high-density non-volatile fast memory using the UV light without the use of any erasing circuitry" for reasons discussed above in relation to independent claim 1.

In regard to independent claim 34, Widdershoven does not disclose "means for erasing the modified flash cell using the UV light without the use of any erasing circuitry" for reasons discussed above in relation to independent claim 1.

Finally, regarding independent claim 35, Widdershoven does not disclose "means for erasing the non-volatile memory by exposing the non-volatile memory to

UV light through the UV light windows without the use of any erasing circuitry" for reasons discussed above in relation to independent claim 1.

Due to the shortcomings of the Widdershoven reference described in the foregoing, Applicant respectfully asserts that Widdershoven does not anticipate Applicant's claims. Therefore, Applicant respectfully requests that the rejection of these claims be withdrawn.

B. Rejection of Claims 33 and 35

Claims 33 and 35 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Kazami et al. ("Kazami," U.S. Pat. No. 5,159,433). Applicant respectfully traverses this rejection.

The Office Action cites the "Background of the Invention" of the Kazami reference for the proposition that independent claims 33 and 35 are anticipated by Kazami. In particular, the Office Action cites column 1, lines 14-18, which provides:

> An EPROM element with an ultraviolet light irradiation window provided in its surface by which it is possible to erase stored data written on a chip by ultraviolet irradiation and rewrite into that memory is preferably used in various types of electronic devices.

In response, Applicant notes that this teaching does not explicitly disclose "erasing the non-volatile memory by exposing the non-volatile memory to the UV light through the UV light windows without the use of any erasing circuitry" as is required by claim 33, or "means for erasing the non-volatile memory by exposing the non-volatile memory to UV light through the UV light windows without the use of

any erasing circuitry" as is required by claim 35. Accordingly, Applicant respectfully submits that the rejection should be withdrawn as to these claims.

II. Claim Rejections - 35 U.S.C. § 103(a)

A. Rejection of Claim 4

Claim 4 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Widdershoven in view of Maayan, et al. ("Maayan," U.S. Pub. No. 2004/0008541). Applicant respectfully traverses this rejection.

As is identified above in reference to independent claim 1, Widdershoven does not teach a memory having no erasing circuitry. In that Maayan does not remedy this deficiency of the Widdershoven reference, Applicant respectfully submits that claim 4, which depends from claim 1, is allowable over the Widdershoven/Maayan combination for at least the same reasons that claim 1 is allowable over Widdershoven.

B. Rejection of Claims 7-8, 16-17, 19-20, and 22-23

Claims 7-8, 16-17, 19-20, and 22-23 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Widdershoven in view of Wu (U.S. Pub. No. 2003/0146465). Applicant respectfully traverses this rejection.

As is identified above in reference to independent claims 5 and 10, Widdershoven does not teach two-terminal drain-gate-connected modified flash cells or memory having no erasing circuitry. In that Wu does not remedy these deficiencies of the Widdershoven reference, Applicant respectfully submits that claims 7-8, 16-17, 19-20, and 22-23, which depend from claims 5 and 10, are allowable over the Widdershoven/Wu combination for at least the same reasons that claims 5 and 10 are allowable over Widdershoven.

C. Rejection of Claims 25-29

Claims 25-29 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Widdershoven in view of Lin (U.S. Pub. No. 2003/0064564). Applicant respectfully traverses this rejection.

As is identified above in reference to independent claim 10, Widdershoven does not teach two-terminal drain-gate-connected modified flash cells or memory having no erasing circuitry. In that Lin does not remedy these deficiencies of the Widdershoven reference, Applicant respectfully submits that claims 25-29, which depend from claim 10, are allowable over the Widdershoven/Lin combination for at least the same reasons that claim 5 10 is allowable over Widdershoven.

D. Rejection of Claim 31

Claim 31 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Widdershoven in view of Kozicki, et al. ("Kozicki," U.S. Pat. No. 6,084,796). Applicant respectfully traverses this rejection.

As is identified above in reference to independent claim 30, Widdershoven does not teach erasing a memory without the use of any erasing circuitry. In that Kozicki does not remedy this deficiency of the Widdershoven reference, Applicant respectfully submits that claim 31, which depends from claim 30, is allowable over the Widdershoven/Kozicki combination for at least the same reasons that claim 30 is allowable over Widdershoven.

IV. New Claims

As identified above, claims 36-44 have been added into the application through this Response. Applicant respectfully submits that these new claims describe an

invention novel and unobvious in view of the prior art of record and, therefore, respectfully requests that these claims be held to be allowable.

CONCLUSION

Applicant respectfully submits that Applicant's pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Alexandria, Virginia 22313-1450, on 9-23-04.

Mary Meegan
Signature